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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,227	01/19/2002	Bruno Kranzen	P05099 (NATHI5-05099)	3911

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10/25/2004

Docket Clerk  
P.O. Drawer 800889  
Dallas, TX 75380

EXAMINER

COTTINGHAM, JOHN R

ART UNIT

PAPER NUMBER

2116

DATE MAILED: 10/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/053,227

Applicant(s)

KRANZEN ET AL.

Examiner

John R. Cottingham

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892) 0
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 12/29/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

### DETAILED ACTION

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-<sup>22</sup><sub>4</sub> are rejected under 35 U.S.C. 102(e) as being anticipated by Maksimovic et al. U.S. Patent 2003/0093160. Maksimovic shows all of the claimed subject matter of a clock control circuitry in Figures 1-15.

Regarding claim 1, Clock control circuitry 200 for selectively applying digital a clock signal to a digital processing component, said clock signal clock signal capable of being changed to a plurality said clock control circuitry operable of operating frequencies (from signal 208 to signal 214), receive a command to change first operating frequency (in clock logic 202, signal Cextclk is changed to signal Ctest 214), in response to said command, disable said applied clock signal (signal 208 does not come out of clock logic 202), generate test clock signal 214 having said second operating frequency, apply said test clock signal 214 to a power supply adjustment circuit 800, and sense a status signal 102 from said power supply adjustment circuit 800 indicating that a power supply level said digital processing component has been adjusted an optimum value suitable for said second operating frequency.

Regarding claim 2, , wherein said clock control circuitry 202 is further operable in response to said status signal to set said applied clock signal to said second operating frequency. (through signal 102 and 226, since the signals are a loop that goes back to the clock logic 202)

Regarding claim 3, wherein said clock control circuitry 202 is further operable to enable said applied clock signal 214. (col. 2, [0033])

Regarding claim 4, further comprising clock divider circuitry 350 and controller 600.

Regarding claim 5, wherein said controller 600 operable disable said applied clock signal 214 response to said received command and enable said applied clock signal response said status signal (102 through data signals from 350).

Regarding claim 6, wherein said clock divider circuitry 350 is operable to generate said test clock signal 214 having said second operating frequency.

Regarding claim 7, further operable to set said applied clock signal 604 to said second operating frequency as a function of said test clock signal and said status signal. Test signal 214 and status signal 102 merge back in 300 to form the applied clock signal 604.

Regarding claim 8, a method of operating clock control circuitry for selectively applying clock signal digital processing component, said clock signal capable being changed plurality of operating frequencies, said method of operating said clock control circuitry 202 comprising the steps of: receiving command change operating frequency 208 to a second operating frequency 214; disabling, in response to said command, said

applied clock signal 208; generating test clock signal 214 having said second operating frequency; applying said test clock signal 214 adjustment circuit 600 ; and power supply 204 sensing a status signal 102 from said power supply adjustment circuit 800 indicating that a power supply level said digital processing component has been adjusted an optimum value suitable for said second operating frequency 214.

Regarding claim 9, further comprising the step of setting, in response to said status signal 208, said applied clock signal 208 to said second operating frequency 214.

Regarding claim 10, further comprising the step of enabling said applied clock signal 208.

Regarding claim 11, wherein said clock control circuitry comprises clock divider circuitry and a controller. (through clock logic 202)

Regarding claim 12, a digital circuit comprising: a digital processing component capable of operating different clock frequencies; an adjustable power supply 800 capable supplying variable power supply level, VDD, said digital processing component; power supply adjustment circuitry capable of adjusting VDD; and control circuitry 202 for selectively applying clock signal said digital processing component, said clock signal 208 capable of being changed to plurality of operating frequencies 214 and 216, said clock control circuitry 202 operable to (i) receive command 226 change a first operating frequency to second operating frequency, response to said command, disable said applied clock signal, (iii) generate test clock signal 214 having said second operating frequency, (iv) apply said test clock signal 214 said power supply adjustment circuit 800, and sense a status signal 102 from said power supply adjustment circuit indicating that

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a power supply level of said digital processing component has been adjusted an optimum value suitable for said second operating frequency.

Regarding claim 13, wherein said clock control circuitry is further operable in response to said status signal 102 and 226 set said applied clock signal 208 said second operating frequency 214.

Regarding claim 14, wherein said clock control circuitry 202 is further operable to enable said applied clock signal.

Regarding claim 15, wherein said clock control circuitry further comprises clock divider circuitry and a controller. (inside 202)

Regarding claim 16, wherein said controller 202 is operable to disable said applied clock signal response said received command and enable said applied clock signal in response to said status signal.

Regarding claim 17, wherein said clock divider circuitry is operable to generate said test clock signal having said second operating frequency.

Regarding claim 18, wherein said clock control circuitry 202 further operable to set said applied clock signal 208 said second operating frequency 214 is function of said test clock signal 214 and said status signal (102 through 226).

Regarding claim 19, further comprising N delay cells 300 coupled in series, each of said N delay cells having a delay D determined by a value of VDD 102, such that a clock edge applied to an input of first delay cell ripples sequentially through said N delay cells.

Regarding claim 20, wherein said power supply adjustment circuitry 214 is operable to (i) monitor outputs of at least a K delay cell and a K+1 delay cell, determine that said clock edge has reached an output of said K delay cell and has not reached an output of said K+1 delay cell, and (iii) generate a control signal capable of adjusting VDD.

Regarding claim 21, wherein said power supply adjustment circuitry is further operable determine that said clock edge has reached said K delay cell output and has not reached said K+1 delay cell output when a next sequential clock edge is applied to said first delay cell input.

Regarding claim 22, wherein a total delay from said first delay cell input to said K delay cell output is greater than a maximum delay of said digital processing component.

### ***Conclusion***


3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Fulmer et al. U.S. Patent 6,498,321, Hallberg et al. U.S. Patent 4231335, and Sonada U.S. Patent 5,914,631 show similar inventions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John R. Cottingham whose telephone number is (703) 306-3439. The examiner can normally be reached on Monday - Thursday, alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571)272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John R. Cottingham  
Primary Examiner  
Art Unit 2116

jrc